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EXAMINER	
STEVENS, THOMAS H	

ART UNIT	PAPER NUMBER
2123	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/804,504	STEWART ET AL.	
	Examiner	Art Unit	
	Thomas H. Stevens	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 March 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 March 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/12/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-23 were examined.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

3. Claim 4 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The examiner requests clarification of following statement: "...wherein the multiplexing subsystem is implemented in a reconfigurable logic system in which the digital logic emulation system is implemented".

4. Claim 1 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The examiner finds the first two sentences confusing such that the question arises, "who or what is doing the responding".

5. Furthermore, claims 11 and 15 , the words "associated/association" renders the claims indefinite because it is unclear whether the limitations following the word(s) are part of the claimed invention. See MPEP § 2173.05(d).

Double Patenting

6. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

7. Claims 1-5 are rejected under the judicially created doctrine of double patenting over claims 1-5 of U.S. Patent 5,802,348 since the claims, if allowed, would improperly extend the "right to exclude" already granted in the patent.

The subject matter claimed in the instant application is fully disclosed in the patent and is covered by the patent since the patent and the application are claiming

common subject matter, as follows: For example Claim 1 (09/804504) discloses logic analysis system for digital logic comprising a clock signal generator and a multiplexing subsystem (lines 1-12) but doesn't teach a plurality of multiplexing circuits with a controller. However, claim 1 of the patent (5,802,348) does teach a logic analysis system for digital logic emulation system comprising a clock signal generator and a multiplexing subsystem for transmitting logic values of logic signals (column 8, lines 18-29). Furthermore, claims 2-5 of the application grammatically match the claims 2-5 listed in the patent.

One of ordinary skill in the art at the time of invention would have known both of these claims are the same by deduction. Therefore, this is double patenting.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 1-10, and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Babb ("Virtual Wires: Overcoming Pin Limitations in FPGA-based Logic Emulation" (MIT 1993)). Babb teaches the concept of Virtual Wires for FPGA-based logic emulation (abstract).

Claim 1. A logic analysis system for a digital logic emulation system (abstract: 1st paragraph;pg.19, Logic Emulation; and section 1.3 pg. 22-23) configured to model a digital system and operating in response to at least one emulation clock signal (pg. 44, section 4.4, 2nd paragraph) the logic analysis system comprising: a clock signal generator for generating a multiplexing clock signal(pg. 44, section 4.4, 2nd paragraph); and a multiplexing subsystem for transmitting logic values of logic signals from the digital logic emulation system to a logic analyzer, the multiplexing subsystem multiplexing multiple logic values on channels of the logic analyzer for cycles of the emulation clock in response to the multiplexing clock signal (pg. 45-46, section 5.1, with figure 5-1 and pg. 51, figures 5-4 and 5-5).

Claim 2. A system as described in Claim 1, wherein the multiplexing clock signal from the clock generator has a frequency that is higher than each one of the user clock signals (pg. 39, section 4.1, 1st bullet).

Claim 3. A system as described in Claim 1, wherein the multiplexing subsystem transmits the multiplexing clock signal to the logic analyzer as a strobe signal (pg. 62, first bullet and lines 8-9).

Claim 4. A system as described in Claim 1, wherein the multiplexing subsystem is implemented in a reconfigurable (pg. 20, line 24 through pg. 21, lines 1-7 with figure 1-2) logic system in which the digital logic emulation system is implemented.

Claim 5.A system as described in Claim 1, wherein the multiplexing subsystem transmits tag signals to the logic analyzer to identify the logic values being transmitted to the logic analyzer (pg. 76-77, section 7.6 with table 7.6.; and pg. 47, section 5.2).

Claim 6. A system as described in Claim 1, wherein the multiplexing subsystem comprises: a multiplexers circuit for receiving and then transmitting the logic values to the logic analyzer; and a controller for controlling the multiplexers circuit to sample the logic signals to obtain the logic values and to transmit the logic values (pg. 46, figure 5.1; pg. 66, lines 2-8 with figure 6.4; and pg.22, figure 1-3).

Claim 7. A logic emulation system including reconfigurable logic devices and an interconnect for transmitting logic signals between the logic devices, and being configured to comprise: a digital logic emulation portion for modeling a digital system operating in response to at least one emulation clock signal (pg. 46, figure 5.1; pg. 66, lines 2-8 with figure 6.4; and pg.22, figure 1-3; and pg.77, section 7.7); and a logic analysis multiplexing portion for transmitting logic values of logic signals from the digital logic emulation portion to a logic analysis device (pgs. 20-22).

Claim 8. A system as described in Claim 7(pg. 46, figure 5.1; pg. 66, lines 2-8 with figure 6.4; and pg.22, figure 1-3; and pg.77, section 7.7), wherein the logic analysis-

multiplexing portion transmits multiple logic values on channels (pg. 32, section 2.3, lines 2,17 and 20) of the logic analysis device for cycles of the emulation clock signal.

Claim 9. A system as described in Claim 7(pg. 46, figure 5.1; pg. 66, lines 2-8 with figure 6.4; and pg.22, figure 1-3; and pg.77, section 7.7), further comprising a clock signal generator for generating a multiplexing clock signal having a higher frequency than the emulation clock signal (pg. 39, section 4.1, 1st bullet).

Claim 10. 10. A system as described in Claim 9(pg. 46, figure 5.1; pg. 66, lines 2-8 with figure 6.4; and pg.22, figure 1-3; and pg.77, section 7.7; pg. 39, section 4.1, 1st bullet), wherein the logic analysis multiplexing portion multiplexes the logic values transmitted to the logic analysis device in response to the multiplexing clock signal.

Claim 20. A method for configuring a logic emulation system including reconfigurable logic devices and an interconnect for transmitting logic signals between the logic devices, the method comprising (abstract: 1st paragraph;pg.19, Logic Emulation; and section 1.3 pg. 22-23): programming the logic emulation system to have a digital logic emulation portion for modeling a digital system operating in response to at least one emulation clock signal(pg. 44, section 4.4, 2nd paragraph); and programming the logic emulation system to have a logic analysis multiplexing portion for transmitting logic values of logic signals from the digital logic emulation portion to a logic analysis device (pg. 22-23, section 1.3).

Claim Rejections - 35 USC § 103

10. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claims 11-13,16-17,19 and 22 are rejected under 35 U.S.C. 103 (a) as unpatentable by Babb ("Virtual Wires: Overcoming Pin Limitations in FPGA-based Logic Emulation" (MIT 1993)) in view of Alexander et al., (U.S. Patent 5,513,338 (1993)). Babb teaches the concept of Virtual Wires for FPGA-based logic emulation (abstract); but doesn't teach sampling specified data values. Alexander et al., teaches methods of sampling data from the emulation of microprocessors.

At the time the invention, it would have been obvious to one of ordinary skill in the art to use Alexander et al to modify Babb since it would have been advantageous for one to have the ability to analyze any portion of the experiment/modeling of circuits for technical anomalies.

Claim 11. A method for sampling digital signals from a digital logic emulation system configured to operate in a digital system having an emulation clock signal (Babb: abstract: 1st paragraph;pg.19, Logic Emulation; and section 1.3 pg. 22-23; pg. 44, section 4.4, 2nd paragraph), the method comprising: sampling selected digital signals within the emulation system (Alexander: column 2 ,lines 18-20); collecting digital signal values associated with the sampled digital signals for cycles of the emulation clock signal (Alexander: column 2 ,lines 18-24); and multiplexing multiple ones of the digital signal values to a logic analysis device for cycles of the emulation clock signal (Babb: pg. 44, section 4.4, 2nd paragraph; Babb: pgs. 20-22;and Alexander: column 2 ,lines 18-24).

Claim 12. A method as described in Claim 11(Babb: abstract: 1st paragraph;pg.19, Logic Emulation; and section 1.3 pg. 22-23; pg. 44, section 4.4, 2nd paragraph; Alexander: column 2 ,lines 18-24), further comprising: generating a multiplexing clock signal; and multiplexing of the digital signal values to the logic analysis device in response to the multiplexing clock signal (Babb: pg.43, section 4.3 with figure 4-.3).

Claim 13. A method as described in Claim 11(Babb: abstract: 1st paragraph;pg.19, Logic Emulation; and section 1.3 pg. 22-23; pg. 44, section 4.4, 2nd paragraph; Alexander: column 2 ,lines 18-24), further comprising: transmitting the multiplexing clock signal to the logic analysis
device; and triggering the logic analysis device in response to the multiplexing clock signal (Babb: pg.43, section 4.3 with figure 4-.3).

Clam 16. A method as described in Claim 11(Babb: abstract: 1st paragraph;pg.19, Logic Emulation; and section 1.3 pg. 22-23; pg. 44, section 4.4, 2nd paragraph; Alexander: column 2 ,lines 18-24), further comprising multiplexing of the digital signal values to the logic analysis device in response to a virtual clock signal of the emulation system.

Clam 17. A method as described in Claim 11(Babb: abstract: 1st paragraph;pg.19, Logic Emulation; and section 1.3 pg. 22-23; pg. 44, section 4.4, 2nd paragraph; Alexander: column 2 ,lines 18-24), further comprising transmitting tag signals to the logic analysis device to identify the digital signal values being transmitted to the logic analysis device (Alexander: column 3, lines 40-45).

Claim 19. A method as claimed in Claim 17(Babb: abstract: 1st paragraph;pg.19, Logic Emulation; and section 1.3 pg. 22-23; pg. 44, section 4.4, 2nd paragraph; Alexander: column 2 ,lines 18-24), further comprising triggering the logic analysis device at least in part in response to the tag signals (Alexander: column 3, lines 40-45).

Claim 22. A digital logic analysis system, comprising: a target system for generating at least one target system clock signal and data signals(abstract: 1st paragraph;pg.19, Logic Emulation; and section 1.3 pg. 22-23); a programmable emulation system for executing a logic design being responsive to the target system clock signal and the data signals and generating data signals to the target system, the emulation system including a clock signal generator for generating a multiplexing clock signal(pg. 44, section 4.4, 2nd paragraph); a logic analysis device connected to the emulation system for sampling logic signals within the emulation system (Alexander: column 2 ,lines 18-20); a configuring device for programming the emulation system to execute the logic design and multiplex logic values of the logic signals to the logic analyzer for every cycle of the target system clock signal in response to the multiplexing clock signal (pg. 22-23, section 1.3).

13. Claims 14,15 and 18 are rejected under 35 U.S.C. 103 (a) as unpatentable by Babb ("Virtual Wires: Overcoming Pin Limitations in FPGA-based Logic Emulation" (MIT 1993)) in view of Alexander et al., (U.S. Patent 5,513,338 (1993)) and in further view of Selvidge et al., (U.S. Patent 5,659,716 (1994)). Babb teaches the concept of Virtual Wires for FPGA-based logic emulation (abstract); but doesn't teach sampling specified data values or methods to demultiplex the signals. Alexander et al., teaches methods of sampling data from the emulation of microprocessors while Selvidge et al., teaches an

interconnect transmission of global links between the partition blocks models which allow demultiplexing.

At the time the invention, it would have been obvious to one of ordinary skill in the art to use Alexander et al. and Selvidge et al., to modify Babb since it would have been advantageous for one to have the ability to analyze any portion of the experiment/modeling of circuits for technical anomalies.

Claim 14. A method as described in Claim 11(Babb: abstract: 1st paragraph;pg.19, Logic Emulation; and section 1.3 pg. 22-23; pg. 44, section 4.4, 2nd paragraph; Alexander: column 2 ,lines 18-24), further comprising demultiplexing (Selvidge et al.: abstract, lines 7-9) the digital signal values received from the emulation system.

Claim 15. A method as described in Claim 14(Babb: abstract: 1st paragraph;pg.19, Logic Emulation; and section 1.3 pg. 22-23; pg. 44, section 4.4, 2nd paragraph; Alexander: column 2 ,lines 18-24), further comprising displaying the demultiplexed signal values(Selvidge et al.: abstract, lines 7-9) in association with the emulation clock signal.

Claim 18. A method as claimed in Claim 17(Babb: abstract: 1st paragraph;pg.19, Logic Emulation; and section 1.3 pg. 22-23; pg. 44, section 4.4, 2nd paragraph; Alexander: column 2 ,lines 18-24; and column 3, lines 40-45), further comprising demultiplexing the logic values(Selvidge et al.: abstract, lines 7-9) in response to the tag signals and aligning the logic values to correspond to cycles of the emulation clock signal.

Claim 21. A method as described in Claim 20, further comprising programming the logic emulation system to multiplex multiple logic values on channels of the logic analysis device for every cycle of the emulation clock signal.

14. Claims 23 is rejected under 35 U.S.C. 103 (a) as unpatentable by Babb ("Virtual Wires: Overcoming Pin Limitations in FPGA-based Logic Emulation" (MIT 1993)) in view of Yishay et al., (U.S. Patent 5,548,794 (1994)) . Babb teaches the concept of Virtual Wires for FPGA-based logic emulation (abstract); but doesn't teach a plurality of clock signals during the emulation process.

At the time the invention, it would have been obvious to one of ordinary skill in the art to use Yishay et al., to modify Babb since it would have been advantageous to develop a series of circuits to test parallel processing.

Claim 23. A logic analysis system for a digital logic emulation system(Babb: abstract: 1st paragraph;pg.19, Logic Emulation; and section 1.3 pg. 22-23) configured to model a digital system and operating in response to at least two emulation clock signals, the logic analysis system comprising (Yishay: column 19, claim 5): a clock signal generator associated with each emulation clock signal for generating a multiplexing clock signal in response to the corresponding emulation clock signal; and a multiplexing subsystem associated with each clock signal generator for transmitting logic values of logic signals

from the digital logic emulation system to a logic analyzer, the multiplexing subsystem multiplexing multiple logic values on each channel of the logic analyzer for every cycle of the corresponding emulation clock in response to the corresponding multiplexing clock signal (Babb pg. 22-23).

Correspondence Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mr. Tom Stevens whose telephone number is (703) 305-0365, Monday-Friday (8:00 am- 4:30 pm) or contact Supervisor Mr. Kevin Teska at (703) 305-9704. The fax number for the group is 703-872-9306.

Any inquires of general nature or relating to the status of this application should be directed to the Group receptionist whose phone number is (703) 305-3900.

July 8, 2004

THS

KEVIN J. TESKA
SUPERVISORY
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